

CLAIMS:

1. An embedded host controller, for use in a USB system comprising a processor and an associated system memory, the host controller comprising:
 - a DMA controller,
 - the host controller being adapted such that, in order to retrieve data from the associated system memory, a starting address and block length are sent to the DMA controller, and
 - the DMA controller being adapted such that, on receipt of a starting address and block length sent from the host controller, it retrieves the indicated data from the associated system memory.
2. An embedded host controller as claimed in claim 1, wherein the DMA controller is adapted to send a bus request to the processor, and to retrieve data from the associated system memory only when bus access has been granted.
3. An embedded host controller as claimed in claim 2, wherein the host controller comprises a programmable register, the programmable register being adapted to store a signal received from the processor indicating a maximum number of clock cycles for which the host controller can occupy the bus during a bus access.
4. An embedded host controller as claimed in claim 3, wherein the host controller is adapted to release the bus on expiry of the maximum number of clock cycles.
5. An embedded host controller as claimed in claim 1, wherein the associated system memory is a SDRAM, and the host controller comprises a SDRAM controller, the SDRAM controller being adapted to perform a refresh function if retrieval of the indicated data from the associated system memory takes longer than a refresh period of the SDRAM.
6. An embedded host controller as claimed in claim 1, wherein the DMA controller is adapted to send a signal to the processor while it is retrieving data from the

associated system memory, thereby preventing the processor from simultaneously attempting to access the associated system memory.

7. A USB host, comprising:

- 5 - a processor, wherein the processor is adapted to grant bus access;
 - a system memory, to which the processor writes USB data; and
 - a host controller, the host controller comprising:
 - a DMA controller, and
 - the host controller being adapted such that, in order to retrieve data from the
- 10 system memory, a starting address and block length are sent to the DMA controller, and
- the DMA controller being adapted such that, on receipt of a starting address and block length sent from the host controller, it sends a bus request to the processor, and retrieves data from the system memory only when bus access has been granted.

15 8. A USB host as claimed in claim 7, wherein the processor is adapted to send to the host controller a maximum duration signal indicating a maximum number of clock cycles for which the host controller can occupy the bus during a bus access, and wherein the host controller comprises a programmable register, the programmable register being adapted to store a maximum duration signal received from the processor.

20 9. A USB host as claimed in claim 8, wherein the host controller is adapted to release the bus on expiry of the maximum number of clock cycles.

10. A USB host as claimed in claim 7, wherein the associated system memory is a

25 SDRAM, and the host controller comprises a SDRAM controller, the SDRAM controller being adapted to perform a refresh function if retrieval of the indicated data from the associated system memory takes longer than a refresh period of the SDRAM.

11. A USB host, comprising:

- 30 - a processor;
- a system memory;
- a sub-system memory, to which the processor writes USB data; and
- a host controller, the host controller comprising:
 - a DMA controller, and

- the host controller being adapted such that, in order to retrieve data from the sub-system memory, a starting address and block length are sent to the DMA controller, and

- the DMA controller being adapted such that, on receipt of a starting address and block length sent from the host controller, it retrieves the indicated data from the sub-

5 system memory,

- the DMA controller being further adapted to send a signal to the processor while it is retrieving data from the sub-system memory, thereby preventing the processor from simultaneously attempting to access the sub-system memory.

10 12. A USB host as claimed in claim 11, wherein the DMA controller is adapted to send a signal to the processor while it is retrieving data from the associated system memory, thereby preventing the processor from simultaneously attempting to access the associated system memory.